## Characterization of Fast Analog-to-Digital Converter (FADC) for Cherenkov Telescope Array

Professor:Prof. Edoardo Charbonedoardo.charbon@epfl.chDoctoral Assistant:Halil Kerim Yildirimhalil.yildirim@epfl.chBarış Can Efebaris.efe@epfl.ch

Project Type:Master/Semester ProjectLocation:Microcity, Neuchatel

Start Date: Flexible

## **Description:**

Analog-to-digital converters are one of the building blocks of many sensor readout circuits. As they provide the interface between analog and digital domains, their performance including noise, sampling speed, power consumption and resolution metrics is critical in complex systems. At AQUA lab we are developing an ADC for an analog silicon photo-multiplier (SiPM) camera readout for gamma-ray detection as a part of the Cherenkov Telescope Array Observatory [1-3] project. Two integrated circuits (IC) were designed, in 110nm and 65nm technologies, based on flash and time interleaved successive approximation register (TI-SAR) architecture. The design has a mixed signal approach consisting of analog core and digital readout/control. The FADC system will be a part of the advanced camera development for the large-scale telescope. The collaborative project includes many contributors across Europe who specialize in different domains from software to hardware of the imaging system. The student is expected to fully characterize the ICs, designing FPGA firmware for data acquisition from hands-on measurements using printed circuit boards (PCBs).

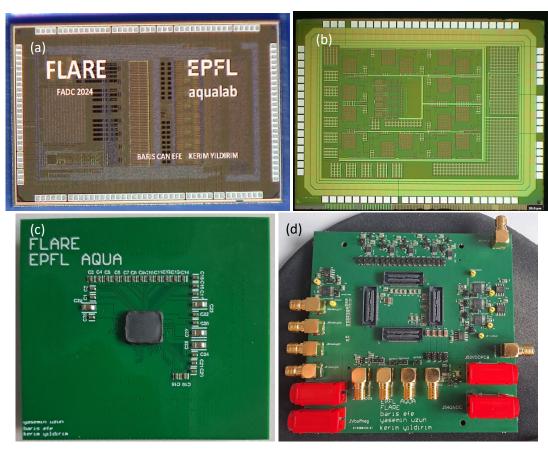


Figure 1. (a) FADC designed in 65nm. (b) FADC designed in 110nm. (c) Packaging of ADC. (d) Test PCB.

## Tasks:

- Literature review on ADCs, comprehensive analysis of taped-out ICs
- FPGA firmware design using Verilog/VHDL to acquire and process ADC raw data
- Software design on Matlab/Python to control FPGA and data post-processing



Project Description

aqualab

• ADC characterization for noise, speed and linearity.

## **Requirements:**

- HDL concepts and design (VHDL or Verilog)
- Understanding the basics of analog circuit design
- Familiarity with IC design
- Matlab/Python programming
- Familiarity with ADC architectures is a plus (not obligatory)
- [1] https://www.ctao.org/
- [2] https://www.unige.ch/sciences/astro/cta/
- [3] https://www.sbfi.admin.ch/sbfi/en/home/research-and-innovation/international-cooperation-r-and-i/international-research-organisations/ctao.html