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PII: S0925-4005(13)00600-X
DOI: http://dx.doi.org/doi:10.1016/j.snb.2013.05.037
Reference: SNB 15525

To appear in: *Sensors and Actuators B*

Received date: 25-2-2013
Revised date: 3-5-2013
Accepted date: 8-5-2013

Please cite this article as: S.C. Kilchenmann, E. Rollo, E. Bianchi, C. Guiducci, Metal-coated Silicon Micropillars for Freestanding 3D-electrode Arrays in Microchannels, *Sensors and Actuators B: Chemical* (2013), http://dx.doi.org/10.1016/j.snb.2013.05.037

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Metal-coated Silicon Micropillars for Freestanding 3D-electrode Arrays in Microchannels

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Abstract

This paper presents a fabrication process for arrays of high-aspect-ratio micropillar electrodes, which are freestanding 3D structures that feature metal sidewalls connected to passivated planar wires. Facing vertical electrodes are considered to be a key solution in microdevice technologies, as they are able to improve the efficiency and accuracy of electrical methods by generating homogeneous electric fields along the height of microfluidic channels. Despite the acknowledged advantages of using vertical microelectrodes, current microfabrication technologies do not allow the manufacture of such structures with the same resolution and versatility as planar electrodes. The present study focused on the fabrication of round and square-shaped silicon pillar arrays exposing metal on their sidewalls, which is decoupled from the substrate by means of a passivation layer. The pillars range in width from 10 µm to 70 µm, with gaps down to 10 µm and a maximum aspect ratio of 5:1. Metal deposition and patterning were revealed to be the critical steps of the process. Deposition was achieved by sputtering, while patterning was performed by photolithography, and the photoresist was applied by spray-coating. The pattern was then transferred into the metal layer by means of dry etching. This new process can be adapted to any metal that is suitable for depositing by sputtering and patterning by dry etching. The presence of the metal layer on the vertical sidewalls was confirmed by SEM imaging combined with EDX analysis. The arrays were then characterized by electrical conductivity measurements and impedance spectroscopy.

Keywords:

Silicon microfabrication, 3D electrodes, microelectrode arrays, Lab-on-a-chip, cell manipulation and analysis

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1 Introduction

Electrical signals have been used for a wide range of applications in microfluidic or lab-on-a-chip devices. Cell and particle counting has been achieved with on-chip coulter counters [1-3], while impedance spectroscopy has been applied to study particles and to extract their electrical parameters [4], and dielectrophoresis has been used to sort and move specific cells and particles depending on their electrical characteristics [5]. Furthermore, electrical fields are used to manipulate cells. The high resolution of microfabrication technologies makes it possible to apply high and localized electric fields that can be used for the electroporation of cells [6, 7]. The same principle can be used to lyse complete cells, as several research groups have shown [8-10]. It has also been shown that cell fusion can be induced through the application of an electric field between two cells [11].

The characteristics of the electrodes play an important role in all of these techniques. The simplest electrode configuration consists of planar electrodes that are deposited on the bottom of microfluidic channels. While the fabrication of such electrodes is easy, this configuration results in heterogeneous fields in the channel. For higher channels in particular, it is hard to reach fields that are strong enough over the whole channel height to be suitable to sense or manipulate particles. Better results can be achieved by placing the electrodes so that they face each other. Such an arrangement means that the induced fields exhibit better linearity in between the electrodes, which makes it possible to achieve improved field homogeneity throughout the channel [12, 13]. Two main configurations lead to facing electrodes. The electrodes can either be placed at the top and bottom of a chamber, or they can be fabricated parallel to the channel's sidewalls. In the first case, the top and bottom electrodes must be fabricated separately on two substrates that must then be aligned and bonded together. Also, packaging for such devices is critical, since the electrical contacts of the chips face one another, making it impossible to simply use wire-bonding.

In the second case, the electrodes are placed parallel to the sidewalls and are fabricated and connected on the same substrate. Such electrodes have been fabricated by such methods as etching microfluidic channels into highly doped silicon [14]. Another approach involves obtaining so-called "vertical liquid electrodes" on the channel sidewalls by electric current injections in the channel by planar electrodes in dead-end chambers placed perpendicular to the main flow [15]. Sidewall electrodes can also be obtained by combining wet etching and metal deposition in order to develop elliptic-like channels with electrodes on their internal surfaces [16]. Furthermore, electrodes were fabricated from polymers such as PDMS that turned conductive by mixing them with metal ions [17] such as gold or silver [18], with carbon black particles [19] or with single and multiwall carbon nanotubes [20].

In the two outlined solutions for realizing facing electrodes, the electrode distance is determined either by the channel width or height. The advantage of freestanding electrodes, on the other hand, is that electrode gaps can be designed with more flexibility. This additional degree of freedom makes it possible to design smaller gaps, leading to higher field strength. Furthermore,

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freestanding 3D electrodes make it possible to increase the sensing volume of a sensor, while keeping the distance between the electrodes and the passing particles small. Accordingly, higher throughput can be achieved without affecting efficiency or performance. Moreover, applied potentials can be reduced while achieving the same field strengths.

Freestanding pillar electrodes in microfluidic channels will obviously introduce additional flow resistance and lead to flow disturbances that might be critical for some applications. Nevertheless, freestanding pillar electrodes might also be integrated into channel sidewalls [13], if needed, in order to avoid flow disturbances caused by the pillars.

Although freestanding pillar electrodes offer advantages for electrical-based techniques, their implementation entails specific fabrication challenges. Different processes for such structures have been proposed. Electroplating has been used to realize pillar electrodes consisting of metals [21] or conductive polymers [22]. 3D carbon structures have been realized by patterning thick photoresist that was subsequently turned into conductive carbon structures (CMEMS) by means of pyrolysis [23]. Freestanding carbon structures have also been fabricated by replica moulding of carbon black particles into microfluidic devices [24]. 3D MEAs have been fabricated by a method that combines sputtering, laser-scribing and electroplating [25].

All of the above-mentioned technologies have some drawbacks. In the case of electroplating, process parameters must be accurately controlled in order to achieve good surface properties of the structures. Moreover, the geometry of the structures also has an influence on their surface properties, resulting in design constraints. In cases where electroplating is used in conjunction with laser-scribing, the same problems and restrictions arise over the additional fabrication complexity, making it a long and expensive technology. CMEMS are a cost-effective alternative to the above-mentioned technologies, but the resulting carbon structures have a conductivity that is some orders of magnitude lower than similar metal structures. Furthermore, the shrinkage of the precursor during the pyrolysis step must be taken into consideration during the design phase and also limits the types of shapes that can be obtained. Moreover, the shrinkage observed during pyrolysis almost does not affect the bottom of the pillars where they adhere on the substrate. For this reason, the pillars have the original diameter close to the substrate and then shrink with height, making it difficult, especially for smaller pillars, to achieve uniform gap widths over the full channel height.

With replica moulding of carbon black particles, on the other hand, the resolution and design restrictions correspond to the ones related to the fabrication of the micromould masters. The main drawback of this technology is the high resistivity of the electrodes, which are made from a mixture of PDMS and carbon black particles.

The present paper proposes a new fabrication process that is based on the combination of sputtering and evaporation to selectively deposit conductive and insulating layers, either on the entire wafer surface or only on horizontal planes. In this way, silicon pillars are first passivated and then covered with platinum. Horizontal metal layers are patterned by spray coating and dry etching, and the resulting horizontal features are passivated through the evaporation of a silicon dioxide layer. The choice of materials was motivated by the widespread use of these materials for life science applications; however, any conductive material that can be deposited by sputtering can be used for the electrodes and any insulating material that can be evaporated can be used for

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insulation purposes. The fabrication process was optimized for arrays of 50 µm high round and rectangular-shaped pillars with sizes ranging from 10 to 70 µm. Arrays with inter-pillar spacing down to 10 µm were achieved. The main advantages of this fabrication process are good control of geometrical features of the pillars, excellent surface quality of the electrodes and a wide range of possible materials that can be employed.

2 Materials and Methods

2.1 Microfabrication process

The micropillars were obtained on 4” silicon wafers. For this purpose, first a 4 µm positive tone photoresist (thinned AZ 9260) layer was applied by spin coating. The resist was exposed on a mask aligner (Karl Süss MA/BA 6) with a dose of 220 mJ/cm^2. After the resist was developed, the pattern was transferred into the silicon using a Bosch process (Alcatel AMS 200 DSE) targeting a final etch depth of 50 µm. The entire wafer was passivated by chemical vapour deposition (Centrotherm furnace) of either silicon nitride (Si_3N_4 500 nm) or silicon dioxide (SiO_2 1 µm). A platinum layer with a titanium adhesion layer (Ti/Pt 20/200 nm or 20/140 nm) was then sputtered (Pfeiffer SPIDER 600) on the wafer.

For adhesion purposes of a final passivation layer, an additional layer of titanium (20 nm) was evaporated on top of the platinum (Leybold Optics LAB600H). Evaporation was chosen for this specific layer formation in order to avoid depositing titanium on the vertical sidewalls of the pillars where only platinum is meant to be exposed to the solution.

For the patterning of the metal layers, a diluted AZ photoresist (AZ 9260:PGMEA:MEK 4:8:90) was spray-coated in three superposed layers with successive baking steps for each layer (EVG 150). A short treatment with oxygen plasma (30 sec. 500 W, 400 ml/min, Tepla 300) was performed prior to spray coating. The resist was exposed with a dose of about 780 mJ/cm^2 on a standard mask aligner (Karl Süss MA/BA 6) and developed by an automated development system (EVG 150). The pattern was then transferred into the metal layer by dry etching (STS Multiplex ICP). After photoresist removal, an additional cleaning with piranha solution was performed to remove resist residues.

Finally, for the purposes of electrical insulation, a 200 nm thick SiO_2 layer was evaporated on the horizontal surfaces (Leybold Optics LAB 600H).

2.2 Electron microscopy characterization of micropillar arrays

Two different Scanning Electron Microscopes (SEM, ZEISS LEO and ZEISS MERLIN) were used to observe the patterning of the metal layer inside the gaps. For this purpose, we realized arrays of 50 µm high pillars with different shapes (square and round), dimensions (10 µm to 70 µm) and gaps (10 µm to 60 µm).

An Energy Dispersive X-Ray detector (EDX, Oxford Instruments EDX X-MAX) mounted on the ZEISS MERLIN was employed to analyse the material composition of the vertical sidewalls. Data were treated by the AZTEC software (Oxford Instruments).

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2.3 Electrical Characterization

2.3.1 Resistivity of micropillar arrays

Silicon chips featuring sets of five connected round-shaped pillars of different size, spacing and wire width were developed to evaluate the resistivity of connection lines that comprehended metal-coated micropillars and identify the critical features for the proposed technology (Fig. 1). In particular, our purpose was to evaluate the metal thin film continuity between planar wires and vertical pillar sidewalls and the impact that the pillars have on the resistivity, particularly with respect to their dimension and position. The diameter of the pillars varied from 10 µm to 70 µm and the spacing between them ranged from 60 µm down to 10 µm. Each array consisted of five adjacent pillars connected by a metal line of 10 µm, 20 µm or 30 µm in width ending with two opposite pads (indicated as A and B in Fig. 1). On the same layout, test structures consisting of standard horizontal line patterns having a width between 5 µm and 50 µm were fabricated. Measurements of electrical conductivity on the five-pillar arrays were performed in dry conditions with a Keithley 2400 SourceMeter and a Karl Süss PM8 probe station.
The final passivation step of the chip surface, the purpose of which is to insulate the metal wires from an electrolyte solution, was not applied on these chips since measurements were performed in dry conditions.

2.3.2 Impedance spectroscopy

A specific micropillar layout was conceived in order to facilitate the coupling of the chips with a microfluidic channel to perform electrical impedance measurements in wet conditions. Two adjacent 50 µm high micropillars with a width of 40 µm and spacing of 40 µm were located in a 160 µm-large flow channel obtained by bonding a PDMS cover to the chip. The upstream and downstream faces of the micropillars exhibit a rounded shape to improve the hydrodynamic behaviour by reducing the flow perturbation. In this design, each single pillar is connected by a 1 cm long horizontal metal line to a dedicated pad located on the chip border outside of the PDMS-bonded region. The PDMS cover was obtained from an SU-8 mould. The PDMS and chip surface were cleaned with an isopropanol bath for 10 minutes and then bonded by oxygen plasma (100 W, 0.6 mbar, 12 s, Diener Electronics, Femto). Impedance spectroscopy was performed both in dry and wet conditions. The microfabrication process includes the final surface passivation by SiO_2, as described above, in order to insulate the horizontal metal wires from the electrolyte solution. The resulting pillars expose platinum on their vertical surfaces, while the horizontal wires lie underneath an SiO_2 passivation layer.
A PCB was designed to hold the chips and to provide electrical connection. The backside of the chips was connected to ground in order to suppress capacitive coupling between the metal wires on the chip and the silicon substrate. The characterization of the micropillar electrodes was done using an Agilent 4294A Precision Impedance Analyzer (Agilent Technologies, Santa Clara, CA, USA). Data sets were acquired in LabView (National Instruments Corp., Austin, TX, USA) and analysed in Matlab (Mathworks, Natick, MA, USA). The electrical characterization of the pillars inside the channel was performed both in air and in PBS 1X (Phosphate Buffered Saline, Sigma Aldrich) solution. Impedance spectra were obtained over 201 measurement points distributed

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logarithmically between 10^3 Hz and 10^6 Hz, with an excitation signal of 50 mV. In order to identify the equivalent electrical components, data points were fitted in ZView (Scribner Associates, Inc.).

3 Results and discussion

3.1 Microfabrication

Fig. 2a shows uniform metal coverage of the pillar sidewalls and the continuity with the horizontal metal layer constituting the wires. The presence of platinum was further confirmed through EDX analysis of the sidewalls of the pillars (Figs. 2b and 2c). Silicon, platinum and nitrogen peaks were identified. The presence of nitrogen is due to the passivation layer of silicon nitride underneath the metal layer. The Ti peaks could not be measured due to the limited thickness of the layer.

The patterning of metal connections between the pillars was achieved using spray coating. This technique allows for more homogenous coatings, especially for substrates with high topography, since the layer is sprayed uniformly on the entire wafer and therefore does not need to be spread by centrifugal forces [26].

We noted that treating the photoresist coating with oxygen plasma before spray coating and employing freshly deposited clean metal surfaces play an important role in achieving the best adhesion and uniformity of the coating.

Since smaller droplets adhere better to the substrate, the resist was applied accordingly, starting with a low dispense rate (5 μL/sec). Additional resist was then sprayed, increasing the dispense rate at each passage over the wafer up to 60 μL/sec. This procedure was chosen since an increased dispense rate leads to the formation of bigger droplets, which are more favourable for adhering to already deposited resist and also lead to a smoother surface [27].

The wafer was rotated while the spray nozzle was moved over the wafer in order to achieve coverage of all sides of the pillars, but the rotation was kept at low spin speed (20 rpm) to minimize the centrifugal force effects. Nevertheless, photoresist accumulation and inhomogeneity in resist thickness were observed between the pillars and a dependency between gap size and resist accumulation was also observed. Arrays with smaller gaps result in greater accumulation inside the gaps than similar arrays with bigger gaps. This can be explained by two effects. Firstly, more resist is deposited in a small gap, since the ratio of vertical surfaces to horizontal surfaces is higher. Secondly, capillary forces have a greater effect in small gaps than in larger gaps.

To achieve a sufficiently high exposure dose for the full resist thickness in critical regions, the dose had to be increased. While a dose of 210 mJ/cm^2 was sufficient to pattern planar regions, doses up to 780 mJ/cm^2 were needed to pattern into the arrays with smaller gaps. The fact that the patterning of the metal layer of planar regions and arrays was achieved in the same step meant that planar regions were overexposed. Moreover, a gap separating the wafer from the mask resulted during exposure of the resist due to the presence of the pillars. The combination of the gap and overexposure led to an important shrinkage of planar features, particularly the ones located far from the pillars.

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SEM imaging was used to characterize this effect by measuring the shrinkage of planar test structures consisting of 10 lines with nominal width ranging from 5 µm to 50 µm. Fig. 3a shows SEM images of five of the 10 planar metal lines, while Fig. 3b shows the distribution of the shrinkage of this set of lines over 96 measurements. The shrinkage corresponds to an average of 6.52 µm, with a standard deviation of 1.14 µm.
Furthermore, we observed that shrinkage was less evident for gaps between the square-shaped pillars (Fig. 3c) than for the round-shaped pillars (Fig. 3d). This observation agrees with the explanation above, since the spacing between square-shaped pillars is narrower than the round-shaped ones due to larger facing surfaces in the case of square-shaped pillars.

3.2 Conductivity characterization of 3D metal patterns

In order to characterize the quality of the electrical connection between the metal coated pillars and the horizontal wires, we measured the electrical resistance of lines of five round-shaped pillars, connected by a metal wire with a nominal width of either 20 µm or 30 µm. The sets of pillars also differ in diameter (20 µm to 70 µm) and spacing (10 µm to 60 µm).
The measured resistances of the lines with different geometrical features varied between 14 Ω and 90 Ω. Fig. 4 reports the data for lines obtained on two different wafers. The plots report the resistance normalized by the total length of the corresponding array, including the connection lines to the pads (Fig. 1 from point A to point B).
While electrical connection was successfully achieved for each array, the normalized resistance was shown to be mainly affected by the gap size, resulting in higher resistance in cases of smaller gaps. Fig. 4a shows the inter-chip variability (18 chips) of the resistance per unit length plotted vs. the gap size between the pillars. This plot reports the measurements on arrays having the same pillar diameter (30 µm) and line width (20 µm). Normalized resistance ranges from approximately 40 mΩ/µm to 90 mΩ/µm, with a maximal variability of 10 percent. Fig. 4b reports the normalized resistance of lines with different gap sizes, pillar diameter and line width. No relationship can be found between the resistance of the array and the pillar diameter, which ranges from 20 µm to 70 µm. As expected, the resistance decreased when the line width was increased from 20 µm (crosses) to 30 µm (circles).
This analysis only considered the arrays for which the pillar diameter was equal to or larger than the line width. This choice was motivated by the intention to exclude cases in which the electrical current was allowed to circumvent the pillars.
The normalized resistance of the pillar arrays was compared with the normalized resistance of the planar lines implemented on the same chip. We observed an increase of the normalized resistance due to the presence of the pillars, which was maximal for the 10 µm gap and corresponded to about four times the normalized resistance of the planar lines.
Overall, we can conclude that gap size is the main parameter that affects the resistance of the pillar lines. This effect can be explained by considering that the amplitude of the sputtering angle in the gap region is reduced during metal deposition. This leads to a thinner metal layer inside the gaps and on the sidewalls of the pillars.

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3.3 Impedance characterization of micropillar electrodes

Impedance measurements were conducted in both dry and wet conditions to extract the equivalent electrical parameters of the device formed by two micropillar electrodes in solution. From the measurements in dry conditions, it is possible to extract the geometrical capacitance between the micropillars in air, which includes the contribution of the connection lines. Impedance spectra in dry conditions show purely capacitive behaviour (Fig. 5a) and the geometric capacitance can be estimated as 55 pF. The measurements in wet conditions, which are reported on the same plot, show the occurrence of the electrode/solution interface capacitance of the vertical platinum sidewalls.

The impedance spectra of the microelectrodes in solution can be modelled using the equivalent electrical circuit shown in Fig. 5b. The Constant Phase Element (CPEDL) accurately describes the peculiar interfacial double layer capacitance at the electrodes and can be observed at frequencies lower than 10^4 Hz. Frequencies between 4×10^4 Hz and 5×10^5 Hz are dominated by a resistive behaviour, which depends on the solution resistance, R_{buffer}. The parasitic capacitance C_{stray}, which is mainly due to the capacitive coupling between the electrodes, is observed at frequencies higher than 5×10^5 Hz. Finally, an additional element that consists of a parasitic resistance R_{PAR} in parallel with a capacitance C_{PAR} is in series with the electrode impedance. The data obtained were fitted with the described model in ZView (Scibner Associates, Inc.) in order to extract the values of each component. The extracted electrical parameters are fitted with errors below 3 percent, indicating the suitability of this electrical model to represent our samples (Tab. 1).

The presence of a large capacitance at low frequencies can only be attributed to the existence of an electrode/solution interface; this further demonstrates the exposure of the platinum on the pillar sidewalls to the solution. The effective capacitance corresponding to the extracted constant phase element was found to be 1.3 μF/cm^2 following the procedure reported by Brug et al. [28]

4 Conclusion

This paper has presented a new fabrication process to realize freestanding pillar electrode arrays with metal coverage of the vertical sides. The fabrication is based on standard silicon machining technologies, which offers advantages in terms of availability of equipment as well as compatibility with other processes. The fabrication process presented here is CMOS-compatible and could be implemented together with circuits in order to, for example, address the pillar electrodes.

The two most critical steps for the fabrication are the metallization of the vertical sidewalls of the pillars and the patterning of metals in between closely spaced pillars. The presence of the metal was confirmed using different methods, such as imaging, surface analysis and electrical measurements, and was found to form a homogenous layer. The patterning of the metal was performed by spray coating and dry etching the metal. The patterning of arrays with gaps smaller than about 40 μm was found to be challenging and the parameters for the spray coating and the photolithography steps need to be optimized. The minimal possible gap to be patterned into was found to be 10 μm for round-shaped pillars and 20 μm for square-shaped pillars. With the

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proposed technology, therefore, it is possible to develop arrays with pillars that can be addressed one by one, or to realize connected pillars that are on the same lines.
During the patterning of the metal layer, planar features were found to suffer from shrinkage due to high exposure doses and a resulting exposure gap. The topography of the substrate was found to have an influence on the shrinkage. Planar features in low topography regions were found to suffer the most from shrinkage and a mean size reduction of about 6.5 μm was found. However, the high repeatability of the size of the shrinkage makes it possible to compensate for this effect in the design phase of the device. The shrinkage within the gaps depends on the gap dimension and on the pillar shape. Shrinkage was found to be consistently more important for bigger gaps as well as in the case of round-shaped pillars than for square-shaped ones. The smaller gaps lead to higher photoresist accumulation, which means that higher exposure doses need to be applied in order to be able to entirely develop features inside the smaller gaps. Since different arrays were developed in parallel on the same substrate, the photoresist inside larger gaps was overexposed. This effect can be better handled in devices with only one or a few different geometries since the photolithography steps only need to be optimized for a few gap dimensions, which are usually in a similar range.
One of the main advantages for the obtained pillars is their metal coverage and the possibility to use metal connection lines that result in low resistivity of such devices. A lower resistance of the electrodes results in better performance for measuring signals with small amplitude and reduces Joule heating of the medium when the electrodes are used to apply signals. We made use of these two advantages when we recently implemented a particle detector based on impedance spectroscopy that was able to count particles passing in between the electrodes. The same electrodes were used for this device as were used for the impedance measurements in this paper. Thanks to the small resistance of the electrodes, the device was able to detect small impedance changes between the electrodes that were used to count for passing particles [29].
This study developed test structures with five pillars that were connected with lines of different widths in order to characterize the resistance of the pillars and their connection lines. The resistance of these structures was found to be in a range of tens of Ohms. The presence of the pillars was found to increase the resistance values by only four-fold, most of which depended on the gap dimension. In order to achieve low resistance values, the pillars should be connected by lines that run in parallel instead of through the pillars. The resistance of such arrays could be further decreased by using thicker metal layers. The option to build the pillars out of silicon makes it possible to apply only thin layers of expensive metals on the pillar sidewalls. This represents an advantage with respect to other techniques, such as electroplating, in which the resulting pillars are made from one specific conductive material. Furthermore, it is generally challenging with electroplating to achieve both good surface properties and precise geometries. On the other hand, the fabrication process proposed in this paper makes it possible to realize any pillar geometry that is compatible with photolithography and dry etching.
Moreover, the presented technology makes it possible to achieve sharp edges, as opposed to techniques such as CMEMS, which involves shrinkage of the precursor that occurs during pyrolysis.

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In order to achieve good adhesion of the photoresist to the surface, and therefore good and smooth surface coverage, surface properties, resist composition and spray coating parameters must be optimized and controlled adequately during the coating. Nevertheless, apart from spray coating, the fabrication process only requires standard fabrication technologies.
The present paper describes a fabrication process for passivated freestanding 3D silicon pillars coated with metal that are suitable to be employed for various lab-on-a-chip applications. With this fabrication process, it is possible to achieve arrays that consist of high-aspect-ratio pillars exposing metal on their sidewalls and exhibiting well-defined cross-sections.

5 Acknowledgments

The authors would like to acknowledge the Center of Micronanotechnology (CMi) at EPFL for its support and help concerning fabrication issues. In particular, we would like to thank Dr J.B. Bureau for all his help concerning spray coating and Dr. C. Hibert for helping us troubleshoot the process.
This work has been funded by the SNSF (Swiss National Science Foundation) project Bio3D (200021_140554).

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7 Captions

Fig. 1 SEM image of three sets of five round-shaped micropillar electrodes. The micropillars have 30 μm diameter and 20 μm gap in between them. Platinum planar lines from 10 μm to

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30 μm in width (bottom to top) connect each single array from point A to point B, through the five pillars. Metal surfaces were highlighted on the image by colorization of the corresponding regions.

Fig. 2 (a) Section of a 20 μm gap between two 50 μm-high pillars. The colorized SEM picture shows the conformity of the metal layer (Ti/Pt 20/200 nm) on the vertical sides of the pillars and on the gap bottom. Inset: details of the metal layer on the pillar vertical sidewall; (b) Vertical sidewall of a pillar. The region marked by the rectangle has been characterized by SEM-EDX and resulted in the spectrum represented in (c).

Fig. 3 (a) Shrinkage of the planar lines due to photoresist overexposure. Dashed black lines indicate the patterns on the original mask design. (b) Bar chart of measured shrinkage over 96 measurements; (c-d) Patterned connection lines in between pillars for square-shaped pillars with a 20 μm gap and round-shaped pillars with 10 μm gap ((c) and (d), respectively). The nominal width of the lines is 10 μm, 20 μm and 30 μm from bottom to top. Scale bars are 50 μm.

Fig. 4 (a) Inter-chip variability (18 chips) of the resistance of the arrays, normalized by the array length, vs. the gap between pillars. In the case of 10 μm gap, three out of 18 normalized resistance values were found to be substantially higher, thus they were indicated separately on the plot; (b) Resistance of the arrays normalized by the array length, vs. the gap between pillars. Circles represent 30 μm-width lines and crosses represent 20 μm-width lines. Pillar diameter ranges from 20 μm to 70 μm (b).

Fig.5 (a) Impedance modulus and phase of two adjacent micropillar electrodes in dry (solid lines) and wet measurement conditions (dashed line); (b) Equivalent circuit of the two pillars in the microfluidic channel used for fitting; (c) Fit of the experimental data. Only 101 frequency measurement points over 201 are represented in the plot.

Table 1 Values of the electrical parameters for two micropillars electrodes in a microfluidic channel extracted by fitting of the equivalent circuit in Fig. 5b.

8 Vitae

Samuel Kilchenmann received his M.Sc. Degree in Microengineering with a minor in Biomedical technologies from the Ecole Polytechnique Fédérale de Lausanne (EPFL). He is currently pursuing his Ph.D. degree in Biotechnology and Bioengineering at EPFL focusing on the development of electrical measurement techniques to observe the interactions between proteins and cell membranes in real-time.

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Carlotta Guiducci Carlotta Guiducci is an Assistant Professor of Bioengineering and Swiss-up Chair at the Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland (EPFL). She received her PhD degree in Electrical Engineering from University of Bologna (I). From 2005 to 2007, she was a postdoc at the ESPCI-ParisTech, Paris (F). Her research interests include micro and nanosensors for bioanalytics, the selection of DNA aptamers for the detection of small molecules and the development of heterogeneous integration technologies for electronic biochips. Recently, she has been interviewed by the journal “Electronics Letters” on the present and future role of semiconductors in personalized medicine.

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Table 1 Values of the electrical parameters for two micropillars electrodes in a microfluidic channel extracted by fitting of the equivalent circuit in Fig. 5b.

	R_{buffer} Ω	CPE_{DL} (Q) nF	CPE_{DL} (α)	CPE_{stray} pF	R_{PAR} Ω	C_{PAR} pF
Value	12246	1.26	0.88	2.82	7206	0.36
Fitting error %	2.9	1.6	0.2	1.5	0.5	0.3

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Fig1.tif

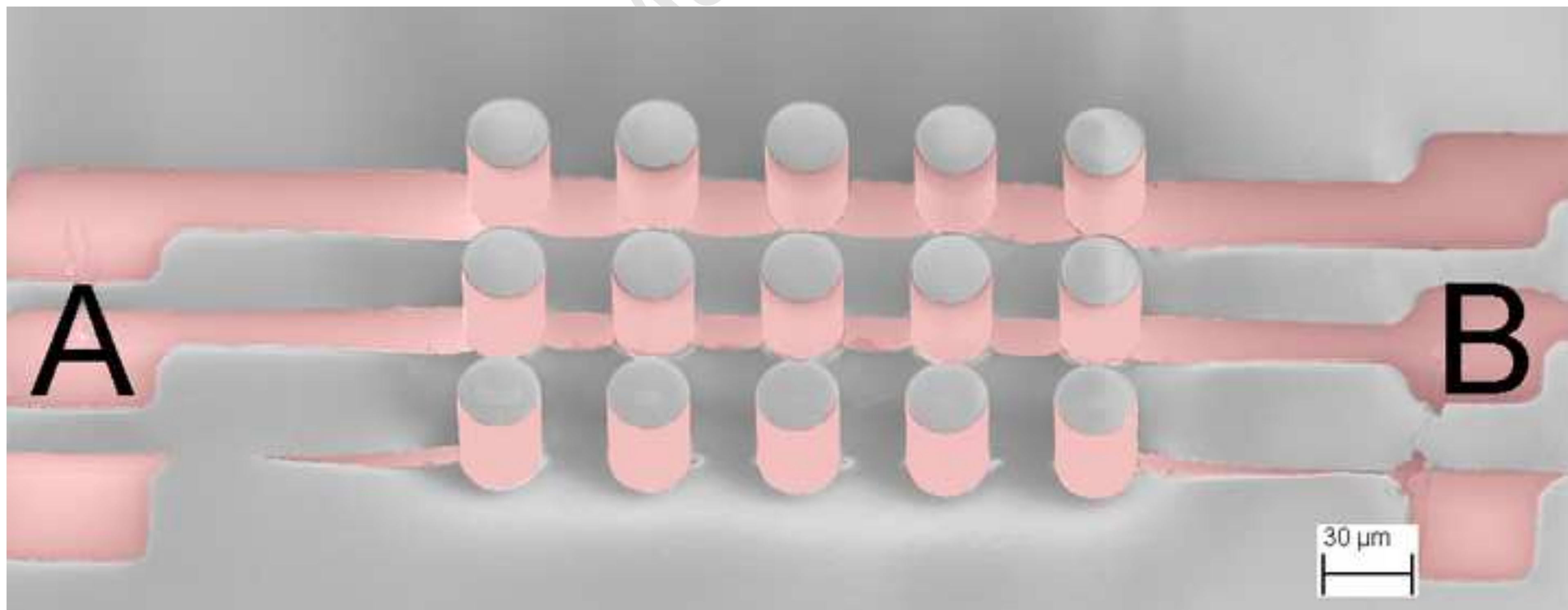

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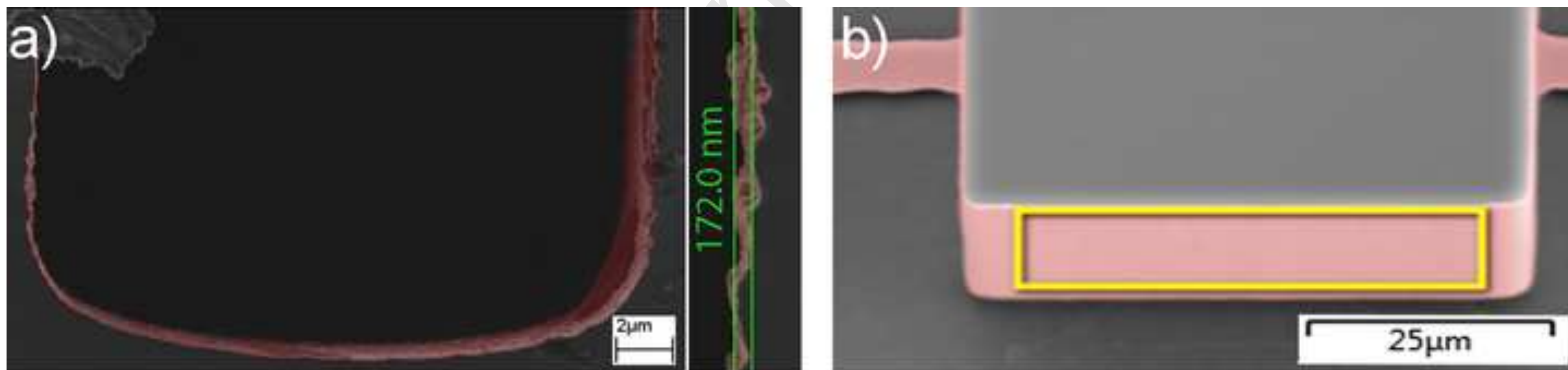
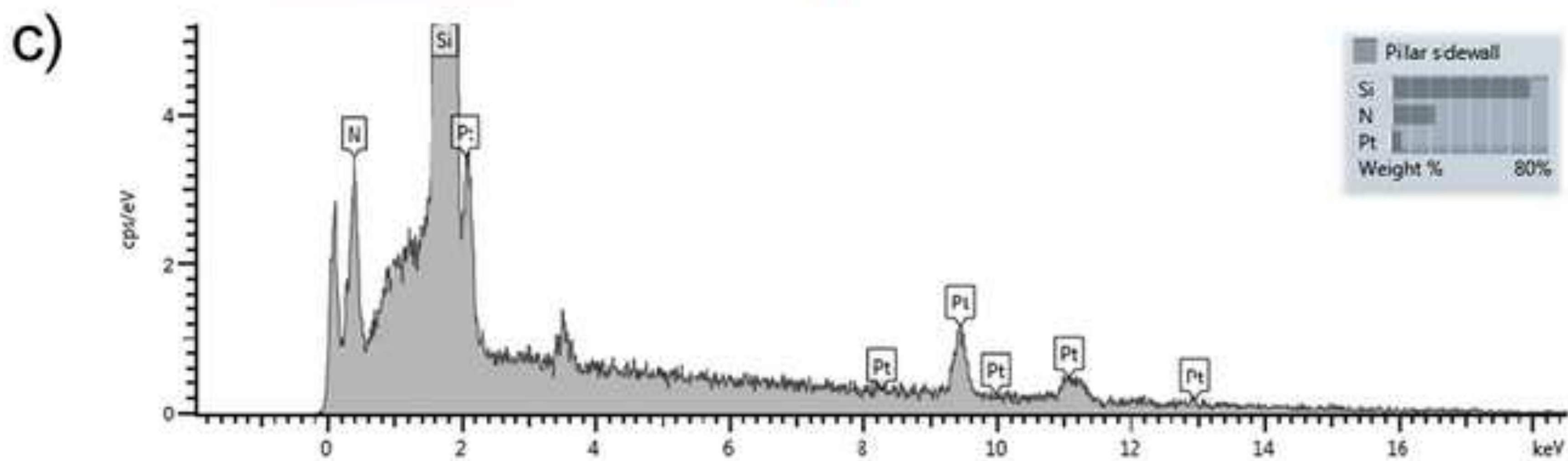
Fig2.tif





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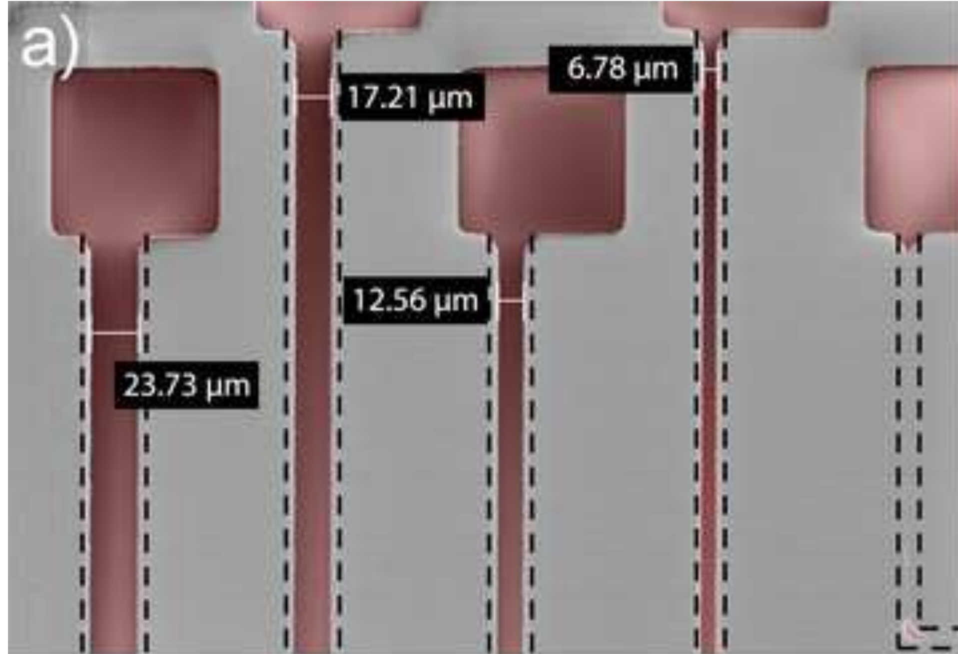

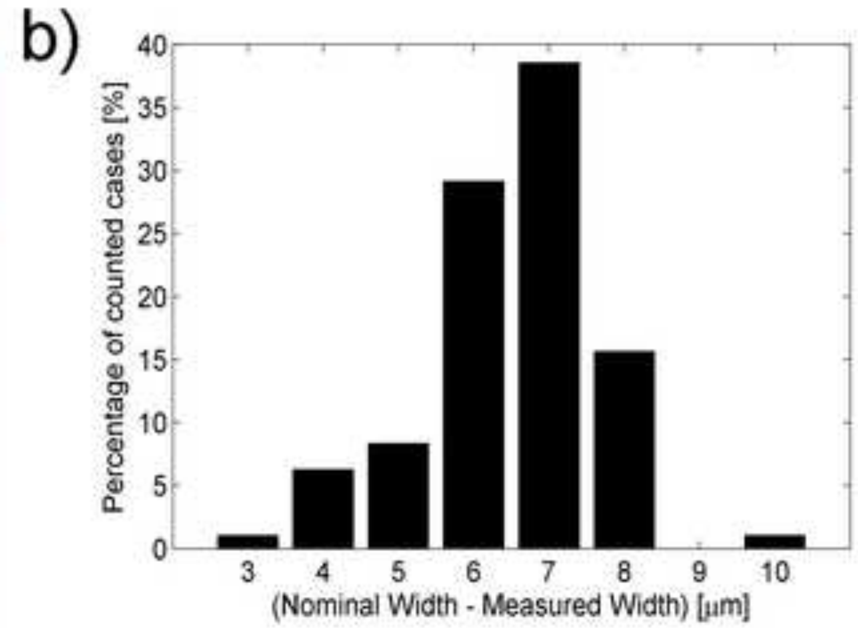

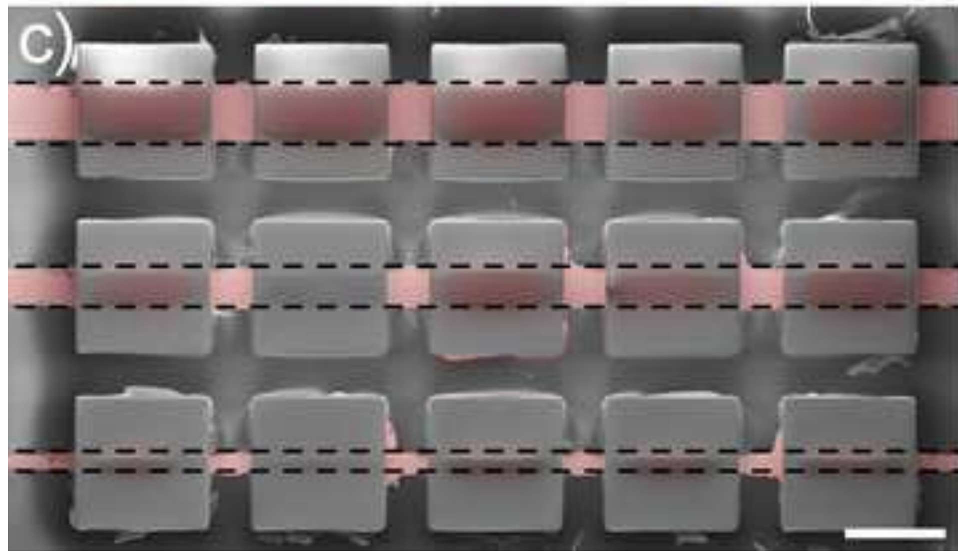

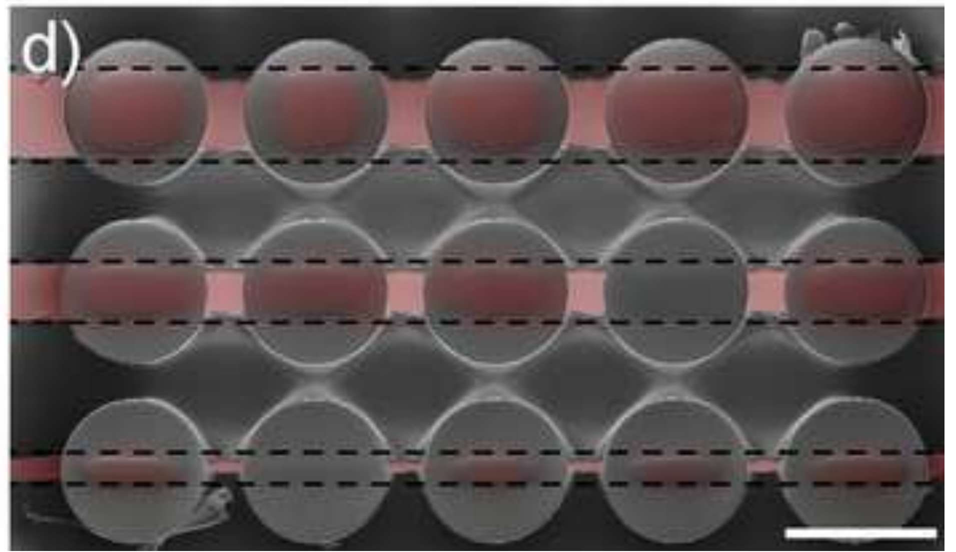

Fig4

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a)

μPillar Diameter [30μm]
Line Width [20μm]

Resistance/Length [mΩ/μm]

200
180
160
140
120
100
80
60

10 20 30 40 50 60

Gap [μm]

b)

× 20μm Line Width
○ 30μm Line Width

Resistance/Length [mΩ/μm]

200
180
160
140
120
100
80
60
40

10 20 30 40 50 60

Gap[μm]

Fig5.eps