3D Stacked Architectures with Interlayer Cooling (CMOSAIC)

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Presentation

To maintain the overall pace according to Moore's law requires an acceleration of packaging development according to recent ITRS reports. Beneficially for the IT industry, mobile device companies have driven 3D packaging development in the past few years but thermal aspects and high density interconnects have been neglected in those applications. While 2D scaling has been used in high performance processors over several decades, the third dimension has not yet been tackled.

Recent progress in the fabrication of through silicon vias (TSV) has opened new avenues for high density area array interconnects between stacked processor and memory chips. Such 3 Dimensional-Integrated Circuits (3D-ICs) are extremely attractive for overcoming the barriers in interconnect scaling, offering an opportunity to continue the CMOS performance trends for the next decade. By integrating a very large System on a Chip (SoC) in multiple tiers, the average distance between system components is reduced, which in turn will improve the performance, but the challenge to remove the heat is multiplied by the number of layers in the integration of the micro-cooling channels between the silicon vias. The reason is that SoCs dissipate on average about 50-100 W/cm^2, which is already challenging on 2D spread out substrates. It is thus safe to claim that "***the future of 3D stacked SoCs crucially depends on providing practical solutions for heat removal***".

Goal

In CMOSAIC, a multi-disciplinary team will jointly conduct experimental research, develop the necessary modeling tools, simulate 3D-IC stacks and test various prototype stacks to develop practical methods for heat removal in high performance 3D-ICs.

Figure 1 depicts a simplified schematic diagram of a 3D-IC with the chips assembled on top of each other and with vertical TSVs between layers. Microchannel cooling elements are etched into the lower face of each chip to remove the heat dissipated locally by each chip. Two different types of coolants will be evaluated for heat removal: a single-phase water-based nano-fluid and an environmentally friendly, two-phase evaporating refrigerant. The temperatures within the 3D-IC system have to remain below 90°C during operation to avoid damage to the chip. The objective of the coolant is to maintain the chip's temperature at or below this value while dissipating heat fluxes per layer up to 100-150 W/cm^2 and targeting an inlet coolant temperature of 30-40°C.

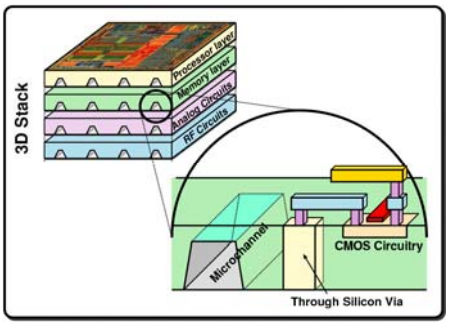

Figure 1. Scheme of target 3D-IC stack

Thus, a very aggressive heat transfer solution is required that involves very high heat transfer rates to the coolant. Most aggressive and most environmentally friendly is a solution where the input temperature is high since this scheme allows direct energy re-use for heating purposes in cold climates. Furthermore, the coolant must function with a low pressure drop (to minimize energy consumption of the cooling system), maintain a near uniform temperature throughout the substrate, avoid passing through the critical heat flux, handle transients in the operating conditions, and cool local hot spots with a 10x higher local power density.

Figure 2 summarizes the overall objective of the project: To build a 3D-IC chip having more than three high power-density logic layers with channels etched on the backside of the chips in between the TSV that provides very large heat transfer coefficients for removal of 100-150 W/cm^2 per layer in between 15x15 mm chips. The 3D-IC is embedded

in a silicon case that provides the manifold structure for fluid input and output and that also allows external contact to a carrier using conventional C4 flip chip bonding. Challenges to build such a system are huge and diverse, requiring development of the TSV etching and plating processes, the channel etching processes, the bonding processes between the layers, the sealing methods, the development of single-phase and two-phase compatible channel network designs, the integration of the chip stacks into a sealed case, the connection to the carrier, and a fluid delivery system.

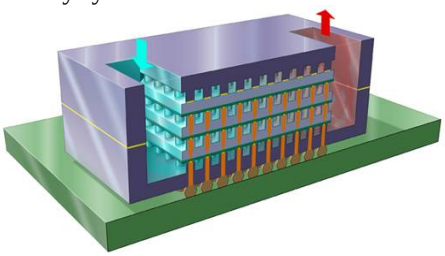

Figure 2. 3D-IC with TSVs and inter-layer cooling channels that is enclosed in a sealed manifold.

The cooling system design involves modelling and optimization of the cooling element, the number and geometry of micro-channels in the substrates, the inlet and outlet fluid ports, and integrating the manifold. While LTNT & FML of the ETHZ and LTCM of the EPFL are world leaders on these two topics, respectively, no definitive thermal models are available for this application and hence are research topics in this project. Once all the input information and boundary conditions are known, the entire 3D-IC stack temperature distribution together with its cooling elements is calculated, including thermal stresses. For the architecture design, modeling at the circuit level, fabrication of the 3D stack and thermal simulations of the microprocessor heat flux "footprints", the LSM and ESL of the EPFL and our industrial partner IBM are world leading specialists.
Figure 3 shows an implementation of the already manufactured instance of 3D stack, which is being used by ESL and LSM to thermally characterize these new architectures. Precisely, this is where the importance of the close interaction between all the groups in this Nano-Tera project comes into play: A final system is electro-thermally co-optimized between the maximal electrical performance and the best cooling performance.

This project addresses the aspect of system integration with two orders of magnitude higher complexities, represented by going from 2D to 3D and from the linking of local IC heat generation to local heat dissipation, and by developing the fundamental understanding, methods and tools required for reliable design of true 3D systems.

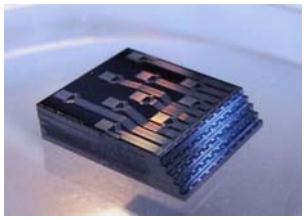

Figure 3. Manufactured 3D -stack in CMOSAIC

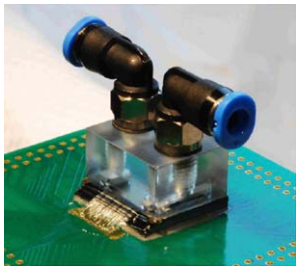

Figure 4.3D-stack enclosed in sealed manifold with inter-layer cooling manufactured in CMOSAIC

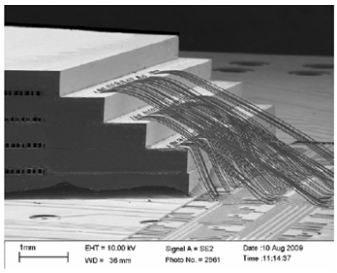

Figure 5. Side view of the wire-bonding process of the 5-tier 3D stack

Furthermore, it will achieve the research objectives of the Nano-Tera.ch program in the field of micro/nano-electronics and the integration of these technologies into high performance computing. Additionally, the proposal specifically matches the Nano-Tera.Ch program's desired characteristics: engineering of complex (tera) systems out of small (nano/micro) components, by leveraging scientific and technological discoveries, with the objective of developing technology demonstrators that can be transformed into products in the medium term, incorporating various disciplines through well coordinated research efforts to explore the proposed topics at the boundary of traditional scientific domains and benefiting the environment.

Overall, from a global perspective, CMOSAIC addresses the vertical axis of micro/nanoelectronics, particularly the aspect of system integration. Specifically, the results of this project will be a significant step toward "***achieving system complexities that are two-to-three orders of magnitude higher than today's state-of-the-art***", by developing the fundamental understanding, methods and tools required for efficient and reliable design of true 3D integrated circuits systems.

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