

Liquid crystal displays using the hybrid alignment method

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ABSTRACT

We describe a new approach for the fabrication of highly integrated low-cost displays based on liquid crystal on silicon (LCOS) technology. The method employs a liquid crystal modulator structure built directly on top of a VLSI die and is suitable to both head-mounted and projection displays.

Keywords: Liquid crystal, silicon backplane, hybrid-aligned nematic, analog modulation, high integration.

1 OVERVIEW OF APPROACH

Our approach for the fabrication of highly integrated displays rests on the use of silicon VLSI backplanes.¹⁻⁴ Substantial costs savings can be obtained by taking advantage of a mature commercial VLSI process. The modulator structure is assembled directly on top of the silicon die (figure 1). The individual pixels of the display are defined by conventional fabrication procedures performed by a commercial foundry. Electrodes made of one of the native metalization levels of the VLSI process are employed as optical mirrors, as well as to apply voltages locally across the liquid crystal layer.

The reflective modulators form an active matrix display. As is the case with the more common transmissive displays, a gating transistor and a storage capacitor are typically associated with each pixel, in order to maintain a satisfactory signal level even when the row in which the pixel is located is not being addressed. The main difference lies in the technology employed to fabricate these transistors. Most active-matrix display panels employ thin-film transistors made of polycrystalline or amorphous silicon. Despite tremendous progress in the last several years, because of yield problems, the fabrication of such transistors remains considerably more expensive than that of MOSFETs on bulk crystalline silicon. While the price and yield gap between thin-film and bulk transistors can be expected to be bridged to some extent over the coming years, VLSI MOSFETs on the surface of silicon dies will retain a significant cost advantage. Therefore, the use of a silicon VLSI backplane provides an opportunity to tap on the high reliability and yields and low cost of mature bulk silicon electronics.

A related benefit of silicon VLSI backplanes is the prospect of compactly and inexpensively integrating elec-

tronics for driving liquid crystals on the backplane, using the same fabrication process employed for the gating transistors. In transmissive active matrix displays, thin-film pixel transistors are fabricated on one of the glass substrates of the liquid crystal cell, while the electronics responsible for refreshing the display are grouped into one or several integrated circuits that are bonded to the substrate containing the pixel transistors. By contrast, a display employing a silicon VLSI backplane can incorporate a number, if not all, of these functions monolithically on the same silicon substrate, in the periphery of the pixel array. The additional cost of these functions is small compared to that of a large pixel array. Since all the necessary electronics can be implemented in an ordinary VLSI process, such highly integrated backplanes would not only enable compact display panels, but also benefit from the high yields, and thus low costs, commonly achieved by mainstream semiconductor processes.

The high-density integration made possible by a VLSI backplane enables the incorporation of additional electronics not only in periphery of the pixel array, but within each pixel. For example, pixel circuitry that provides more constant and better DC-balanced driving signals than the one-transistor "dynamic" circuit has been demonstrated,^{1,5} at the cost of a decreased areal density. Moreover, "smart" pixels are made possible by the integration of many transistors within each pixel; the resulting devices are no longer limited to displays, but can perform advanced functions in various optoelectronic information storage and processing system. For example, Caltech has recently demonstrated an optoelectronic integrated circuit (OEIC) designed to help store and refresh dynamic holograms in compact volume holographic memory systems.⁶ The device can be employed as an electrically or optically addressed latching spatial light modulator (display) and as an optical detector array. Each pixel contains 20 transistors (including a phototransistor) that implement a thresholding optical detector with a programmable threshold level, a static memory bit, an analog multiplexer and various signal gating and buffering functions. In the periphery of the main array are an oscillator that generates the main timing signal required by the IC, a programmable prescaler, microprocessor data bus buffers and drivers, address decoders and three analog multiplexers that generate the waveforms to be applied to the cover glass and to pixels storing ones and zeros, in such a way that all pixels are driven with DC-balanced waveforms, as required for a long display lifetime.

2 FABRICATION OF MODULATORS; ELECTRO-OPTIC RESPONSE

Various methods have been proposed for fabricating liquid crystal modulators on the surface on silicon VLSI dies. While they are differentiated by the type of liquid crystal they employ and by fabrication details, the essence the procedure is as follows (see figure 1). A glass plate coated with a transparent conductor (usually indium-tin oxide or ITO) and with a thin film capable of suitably aligning the liquid crystals, is attached to the surface of the die. It is set at a distance of 1 μm to 10 μm above it by a mixture of UV-cured adhesive and microscopic spacers (for example, chopped glass fibers or polystyrene microspheres). Alternatively, the protective overcoat of the VLSI process can be employed as a spacer, by selectively removing it from the liquid crystal electrode areas while leaving a layer with the proper thickness everywhere else. A contact is provided to the transparent electrode on the glass plate, which is common to all pixels, and the structure is heated to a temperature above the clearing point of the liquid crystal. The cavity between the cover plate and the die is filled with liquid crystal by capillary action. The device is then cooled down to room temperature according to a schedule that ensures an adequate alignment of the liquid crystal.

While early work employed twisted nematic modulators,¹ most current efforts^{5,7} utilize chiral smectic C liquid crystals in the so-called surface-stabilized conformation,⁸ where a small cell gap (approximately 1 μm for reflective devices with typical SmC* mixtures) breaks the naturally formed helix and endows the liquid crystal film with a spontaneous polarization, which can be coupled to an applied field to reorient the molecules. Such modulators have been successfully employed as displays or spatial light modulators (SLMs), as well as in smart pixel arrays. High-density spatial light modulators based on a surface-stabilized ferroelectric liquid crystal (SSFLC) cell fabricated on a CMOS die are now commercially available.⁹ Several functions have been implemented on SSFLC smart

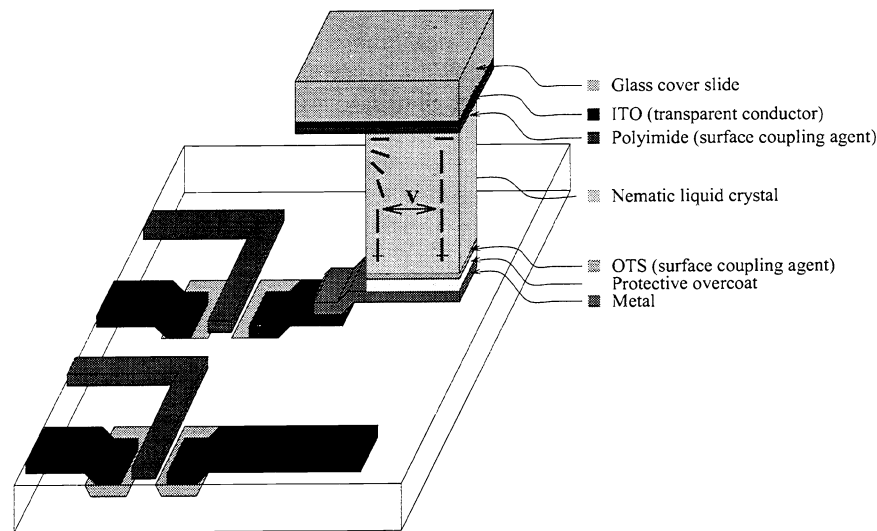


Figure 1: Structure of a HAN-on-VLSI liquid crystal modulator. Other type of liquid-crystal-on-silicon (LCOS) modulators have similar structures.

pixel arrays, including neural plane functions (thresholding,⁴ back-error propagation,¹⁰ winner-take-all¹¹) for optoelectronic neuromorphic systems; such smart pixel arrays detect incoming bi-dimensional optical signals, process the information they represent, and produce an optical bi-dimensional output signal via their liquid crystal modulators. SSFLC modulators provide fast switching, on the order of $40 \mu\text{s}$ at room temperature and low voltages compatible with common VLSI processes. However, their inherent bistability,⁸ which translates into binary optical modulation, can be a problem for some applications requiring true gray-scale modulation. Nonetheless, a few alternative smectic modulator technologies are being actively developed to provide true analog optical modulation while retaining the speed of SSFLC modulators. Two of the main types of materials being investigated for such applications are low-pitch SmC* mixtures for distorted-helix ferroelectric (DHF) modulators, and electroclinic SmA* mixtures. While issues such as alignment quality, temperature stability and low-voltage operation need to be addressed, significant progress is being made.

The alternative to smectic modulators that we have proposed and developed for applications with less stringent speed requirements is the HAN-on-VLSI modulators,^{12,13} which provide analog amplitude or phase modulation at low voltage and frame rates faster than video rate. The modulators employ off-the-shelf, inexpensive nematic liquid crystals; the post-processing performed on the VLSI die that yields the modulator structure is simple and economical, and does not affect the electronic properties of the circuits implemented on the die. The fabrication procedure is as outlined above for a generic liquid-crystal-on-silicon modulator structure, with the following additions. A silane solution is spun on the die before the assembly of the structure, and is baked at 200°C for 30 minutes. The alignment-inducing film on the cover plate is a spun and uniaxially rubbed layer of polyimide, as is common in twisted-nematic and SSFLC modulators.

When no voltage is applied across the cell, the orientation of the nematic director undergoes a smooth transition from horizontal to vertical when going from the top substrate (the cover plate) to the bottom substrate (the die), as a result of the boundary conditions imposed by the aligning films on the substrates (homogeneous alignment on the top substrate, homeotropic alignment on the bottom substrate) and the elasticity of the liquid crystal. In the high-voltage limit (assuming the liquid crystal has a positive dielectric anisotropy), the director is perpendicular to the substrates throughout the cell, and there is no phase retardation between the two eigenmodes excited by a normally incident readout beam. At intermediate voltages, an analog phase modulation is obtained, which can

Electro-Optic Response of Reflective Sample HAN-on-VLSI (5 μm , E7)

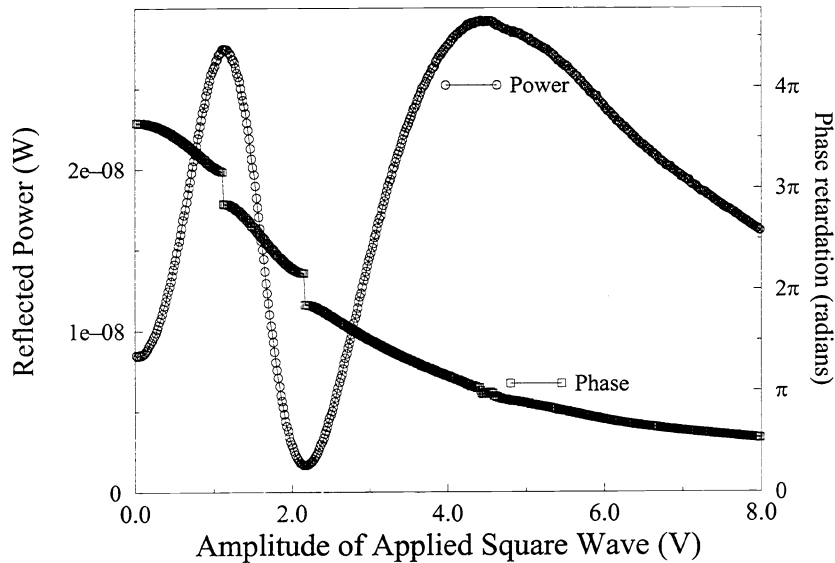


Figure 2: Electro-optic response at 632.8 nm of a HAN-on-VLSI sample employing Merck E7 with a gap of 5 μm .

be converted to amplitude modulation by employing an appropriate combination of polarizer and analyzer (or a polarizing beam splitter).

Figure 2 shows the electro-optic response of such a modulator, showing the reflected power and the inferred phase retardation as a function of the amplitude of the applied DC-balanced square wave. The gap was 5 μm , the cavity was filled with Merck E7¹⁴ and the readout beam had a wavelength of 632.8 nm. The phase retardation of the non-driven modulator is within 8% of the value predicted by theory¹⁵ in the one-constant approximation. Note that unlike twisted nematic and parallel-rubbed cells, HAN-on-VLSI modulators have no noticeable threshold voltage; modulation is already obtained at a driving amplitude of a fraction of a volt. Figure 2 shows that the total reflectance range is spanned by voltages less than 2.1 V, which are compatible with advanced high-density, low-voltage CMOS processes.

3 INTEGRATED CIRCUITS IN DEVELOPMENT

A number of optoelectronic integrated circuits based on HAN-on-VLSI modulators are currently under development at Caltech. One of them is the dynamic hologram refresher (DHR), which was briefly described at the end of §1. The multi-function integrated circuit appears as a RAM mapped in a controlling microprocessor's address space, where groups of eight smart pixels are assembled to form memory bytes. The operation of this device has been demonstrated in a prototype holographic memory system in which holograms of the OEIC display were successfully recorded.⁶

One of the SLM devices is an array of one-transistor pixels with minimal integration of support electronics. Two shift registers address the 110 rows and 72 columns. The display is divided in nine bands of eight columns.

The analog column signals corresponding to eight adjacent pixels are loaded into an eight-channel sample-and-hold circuit that drives the pixels at the intersection of the currently addressed row and band; an external circuit can set up the signals for the next cluster of eight pixels between two samplings. A companion chip containing an array of matched digital-to-analog converters has been designed and fabricated to drive the sample-and-hold circuit on the gray-scale display integrated circuit as well as its cover plate.

A second display features a more advanced integration of control and driving functions and a more accurate control of pixel voltage values, at the cost of a decreased pixel density. The array is comprised of 30 rows and 70 columns. The 70 columns are divided into seven bands of ten columns each. The 10 pixels addressed at any one time can be driven with analog voltages provided by external circuitry, much in the way of the device described above, or by an array of 10 on-chip digital-to-analog converters (DACs). The same die also integrates analog multiplexers that drive the cover plate and dynamically set the upper and lower reference voltages of the DACs to ensure proper DC-balancing of the pixel waveforms. Figure 3 shows the die, with the main pixel array and the group of 10 switched-capacitor DACs clearly visible. Figure 4 shows some letters of the alphabet displayed on the dynamic hologram refresher integrated circuit.

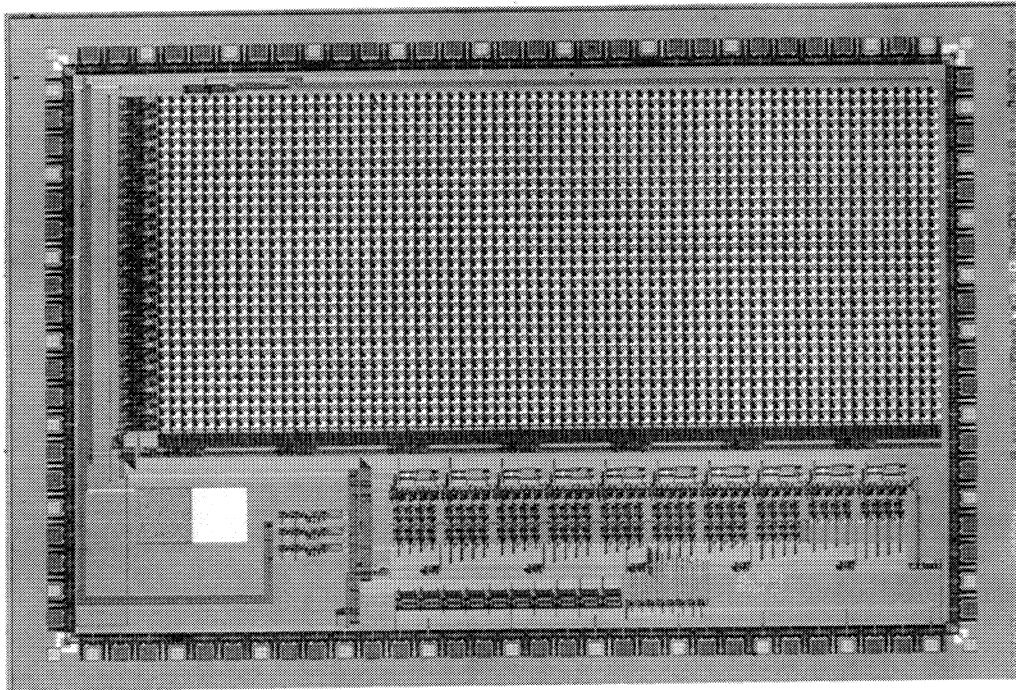


Figure 3: Spatial light modulator die.

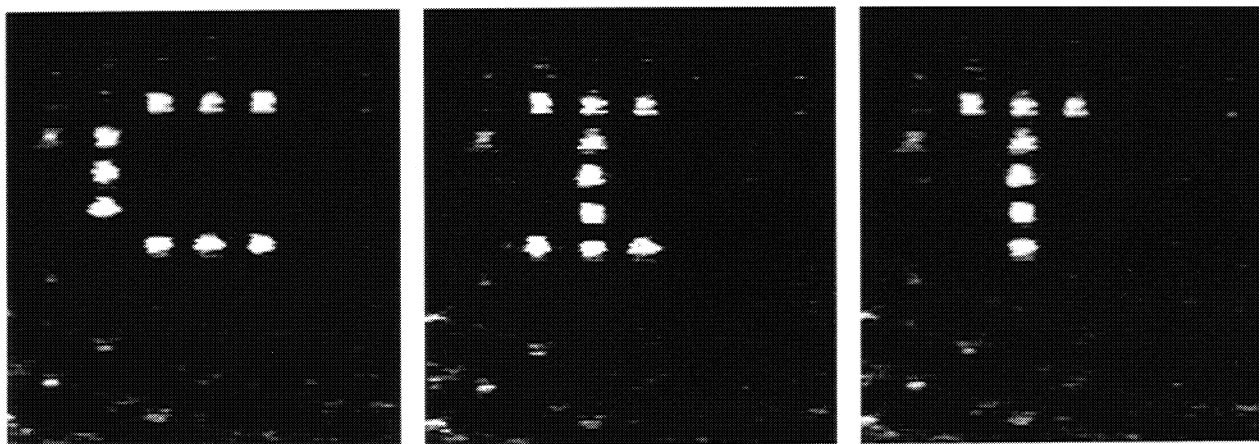


Figure 4: The letters C, I and T displayed on a portion of the dynamic hologram refresher OEIC.

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